CLAIMS:

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1. A data processing device (1) which includes a circuit (2) which consists of various circuit sections (11, 15, 17, 20, 23, 30) which can be fed with a supply voltage (V) via a configuration of conductors (3), and
includes data processing means (17) which constitute such a circuit section that can be fed with the supply voltage (V) and are arranged to process data (DA) while utilizing a characteristic value (CV), and also
includes sequencing means (15) which also constitute such a circuit section that can be fed with the supply voltage (V) and are arranged to execute an algorithm (P) in order to control the data processing means (17) in conformity with this algorithm (P), which algorithm comprises a given number N of sub-algorithms (PB1, PB2, ... PBN) which contain identical sequences of algorithm steps (CO1, CO2, ... COR) and can be executed in a given order each time when the algorithm (P) is executed, and
wherein, upon processing of data (DA) by means of the data processing means (17) under the control of the sequencing means (15) in conformity with the algorithm (P), the data processing causes a current peak pattern to occur at the area of the configuration of conductors (3), the pattern configuration of the current peak pattern being dependent on the algorithm steps (CO1, CO2, ... COR), on the processed data (DA) and on the characteristic value (CV),
characterized in that the circuit (2) additionally includes order fixation means (29) which co-operate with the sequencing means (15) and whereby, upon each execution of the algorithm (P), an order can be fixed from a plurality of feasible orders for the execution of the N sub-algorithms (PB1, PB2, ... PBN).

2. A data processing device (1) as claimed in Claim 1, characterized in that the order fixation means (29) include a random number generator (~~30), and~~
that, by means of the order fixation means (29) upon each execution of the algorithm (P), an order for the execution of the N sub-algorithms (PB1, PB2, ... PBN) is fixed, said order being defined by a random number (Z1, Z2, Z3) generated by the random number generator (30)

3. A data processing device (1) as claimed in Claim 2, characterized in that

the order fixation means (29) additionally include order selection means (33) which contain feasible orders for the execution of the N sub-algorithms (PB1, PB2, ... PBN) and co-operate with the random number generator (30), and

that the order selection means (33) can select an order from the feasible orders in conformity with a random number (Z1, Z2, Z3) received from the random number generator (30).

4. A data processing device (1) as claimed in Claim 1, characterized in that there are provided storage means (20) which co-operate with the sequencing means (15) and in which the algorithm (P) is stored in the form of a program which contains N program blocks as sub-algorithms (PB1, PB2, ... PBN) containing program instructions as algorithm steps (CO1, CO2, ... COR).

5. A data processing device (1) as claimed in Claim 1, characterized in that there is provided a wired logic circuit which co-operates with the sequencing means and contains the algorithm in wired and hence hardware form.

6. A data processing device (1) as claimed in Claim 1, characterized in that the data processing means (17) are formed by means for the encryption and/or decryption of data.

7. A data processing device (1) as claimed in Claim 1, characterized in that the data processing device (1) is formed by a data carrier whose circuit (2) is constructed in integrated technology.

8. A circuit (2) for a data processing device (1)

which circuit consists of various circuit sections (11, 15, 17, 20, 23, 30) which can be fed with a supply voltage (V) via a configuration of conductors (3), and

which circuit includes data processing means (17) which constitute such a circuit section that can be fed with the supply voltage (V) and are arranged to process data (DA) while utilizing a characteristic value (CV), and also

includes sequencing means (15) which also constitute such a circuit section that can be fed with the supply voltage (V) and are arranged to execute an algorithm (P) in order to control the data processing means (17) in conformity with this algorithm (P), which algorithm comprises a given number N of sub-algorithms (PB1, PB2, ... PBN) which contain identical sequences of

algorithm steps (CO1, CO2, ... COR) and can be executed in a given order each time when the algorithm (P) is executed, and wherein,

upon processing of data (DA) by means of the data processing means (17) under the control of the sequencing means (15) in conformity with the algorithm (P), the data processing causes a current peak pattern to occur at the area of the configuration of conductors (3), the pattern configuration of the current peak pattern being dependent on the algorithm steps (CO1, CO2, ... COR), on the processed data (DA) and on the characteristic value (CV),

characterized in that

the circuit (2) additionally includes order fixation means (29) which co-operate with the sequencing means (15) and whereby, upon each execution of the algorithm (P), an order can be fixed from a plurality of feasible orders for the execution of the N sub-algorithms (PB1, PB2, ... PBN).

9. A circuit (2) as claimed in Claim 8, characterized in that

the order fixation means (29) include a random number generator (30), and

that by means of the order fixation means (29) upon each execution of the algorithm (P), an order for the execution of the N sub-algorithms (PB1, PB2, ... PBN) random number (Z1, Z2, Z3) generated by the random number generator (30).

10. A circuit (2) as claimed in Claim 9, characterized in that

the order fixation means (29) additionally include order selection means (33) which contain feasible orders for the execution of the N sub-algorithms (PB1, PB2, ... PBN) and co-operate with the random number generator (30), and

that the order selection means (33) can select an order from the feasible orders in conformity with a random number (Z1, Z2, Z3) received from the random number generator (30).

11. A circuit (2) as claimed in Claim 8, characterized in that

there are provided storage means (20) which co-operate with the sequencing means (15) and in which the algorithm (P) is stored in the form of a program which contains N program blocks as sub-algorithms (PB1, PB2, ... PBN) containing instructions as algorithm steps (CO1, CO2, ... COR).

12. A circuit (2) as claimed in Claim 8, characterized in that

there is provided a wired logic circuit which co-operates with the sequencing means and contains the algorithm in wired and hence hardware form.

13. A circuit (2) as claimed in Claim 8, characterized in that the data processing means (17) are formed by means for the encryption and/or decryption of data.

14. A circuit (2) as claimed in Claim 8, characterized in that the circuit (2) is intended for a data processing device (1) which is formed by a data carrier, and that the circuit (2) is constructed in integrated technology.